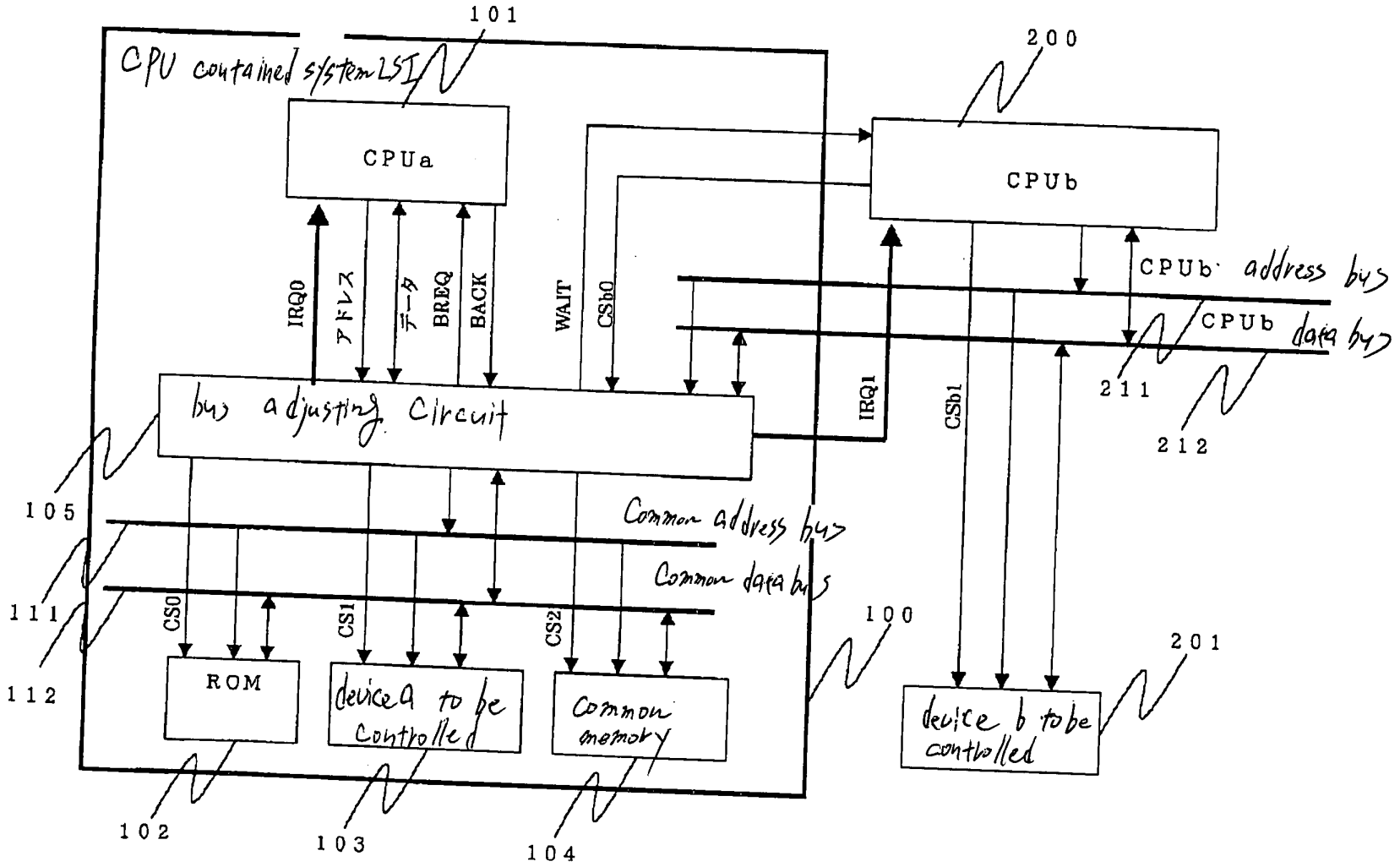

101
CPU contained system LSI
CPUa
CPUb
200
IRQ0
アドレス
データ
BREQ
BACK
WAIT
CSb0
IRQ1
CSb1
CPUb address bus
CPUb data bus
211
212
bus adjusting circuit
105
Common address bus
Common data bus
111
112
CS0
CS1
CS2
100
201
ROM
device a to be controlled
common memory
device b to be controlled
102
103
104

Fig. 1

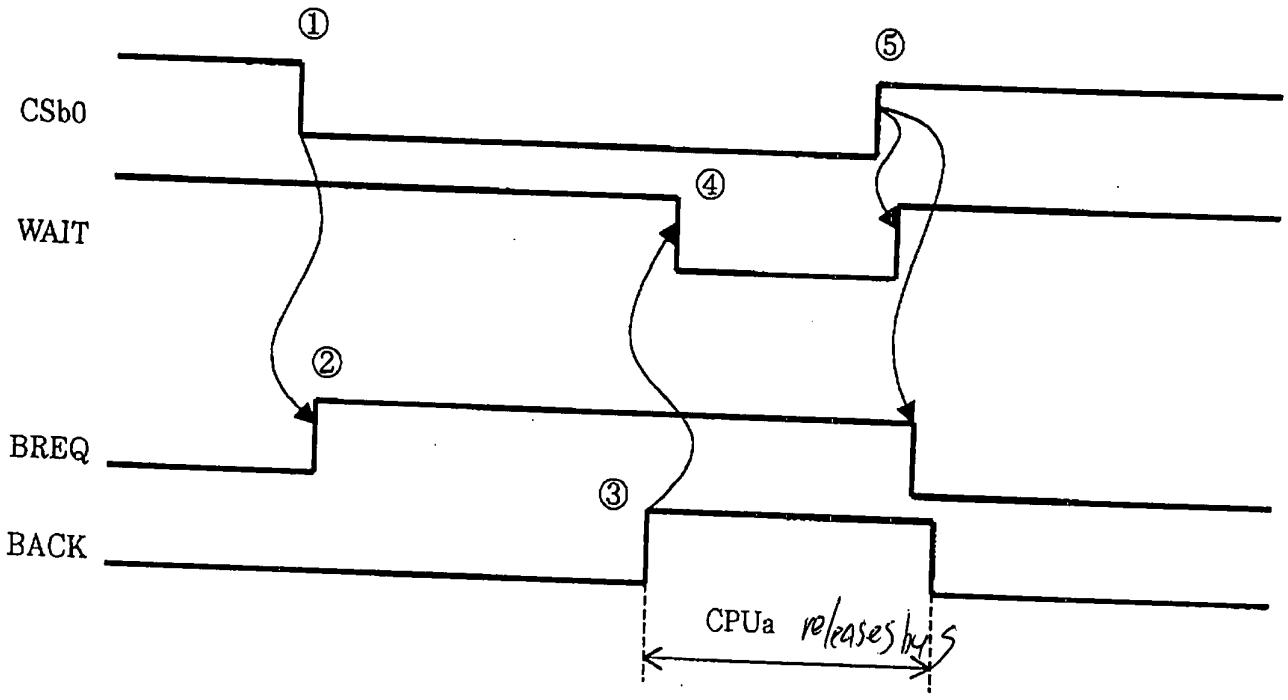
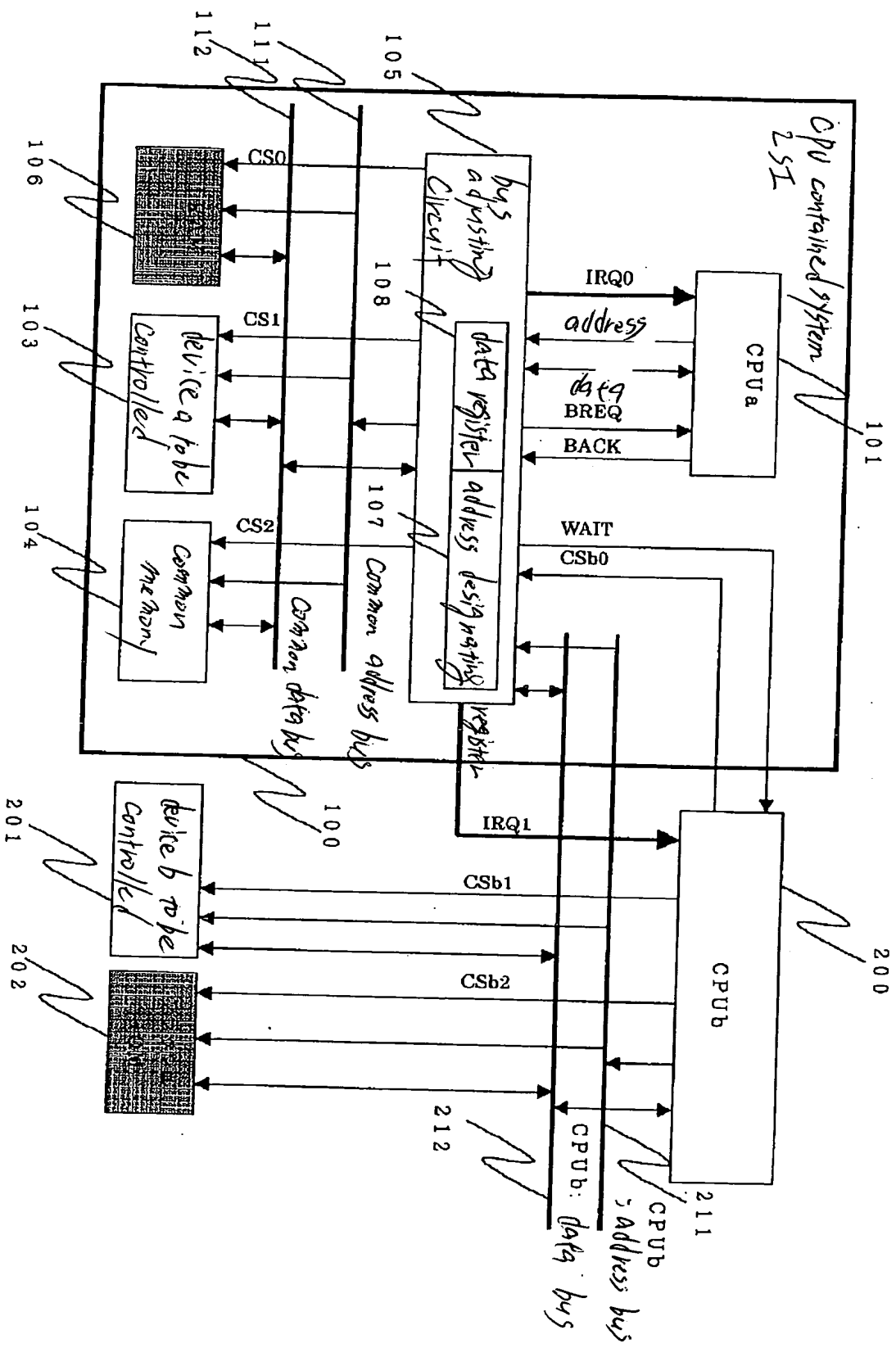
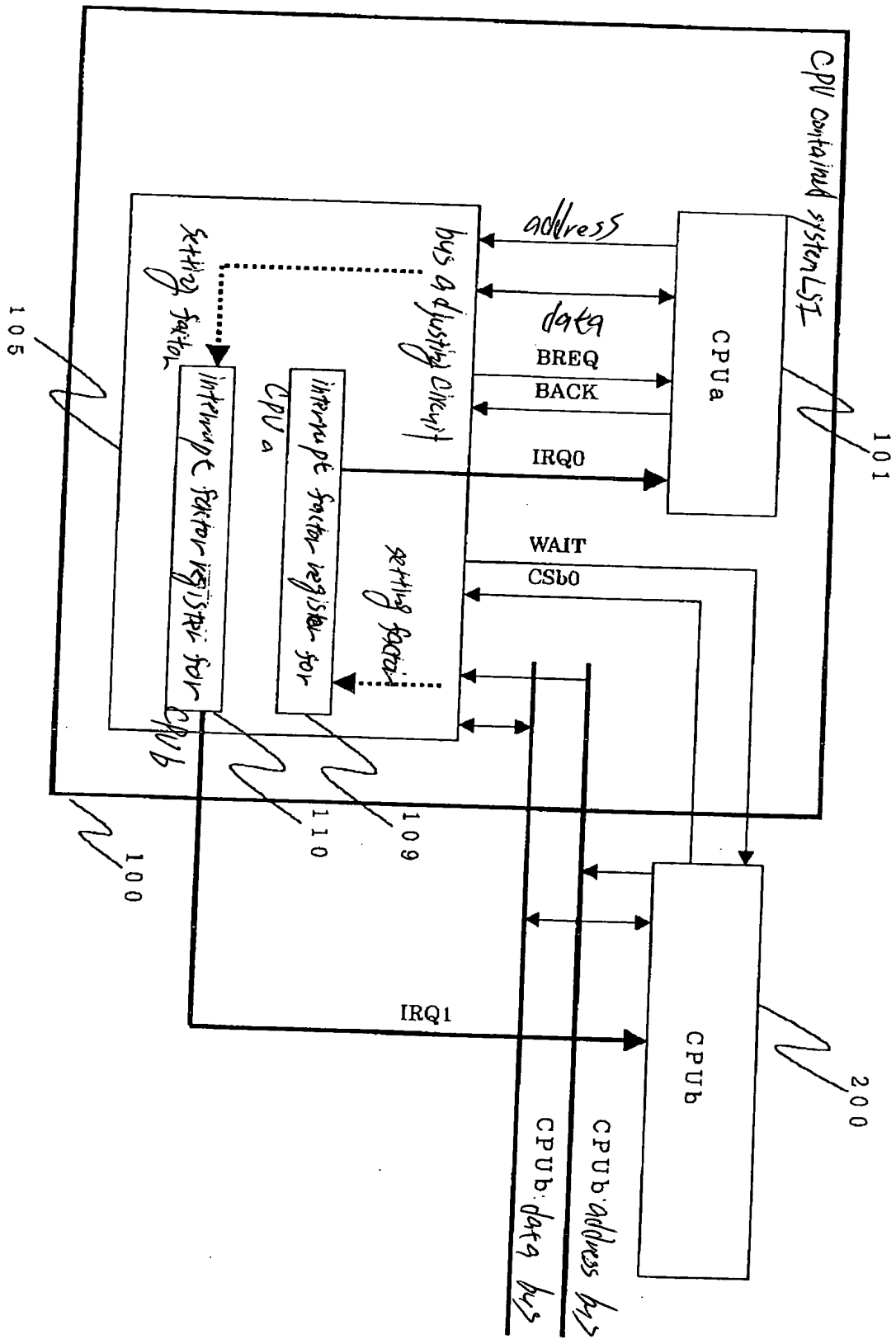


Fig. 2

Fig.3


CPU contained system LSI
101
CPUa
IRQ0
address
data
BREQ
BACK
WAIT
CSb0
IRQ1
CSb1
CSb2
CPUb
200
211
CPUb: address bus
CPUb: data bus
212
bus adjusting circuit
108
data register
address designating
register
105
common address bus
107
common data bus
100
CS0
CS1
CS2
device a to be controlled
103
common memory
104
device b to be controlled
201
202
106
111
112

[Fig. 4]


CPU contained system LSI
bus adjusting circuit
address
data
BREQ
BACK
IRQ0
CPUa
101
WAIT
CSb0
setting register
interrupt factor register for CPU a
setting factor
105
interrupt factor register for CPU b
110
109
100
IRQ1
CPUb
200
CPUb address bus
CPUb data bus

interrupt factor register

Bit0	Bit1	Bit2	Bit3	· · ·	Bit n-1	Bit n

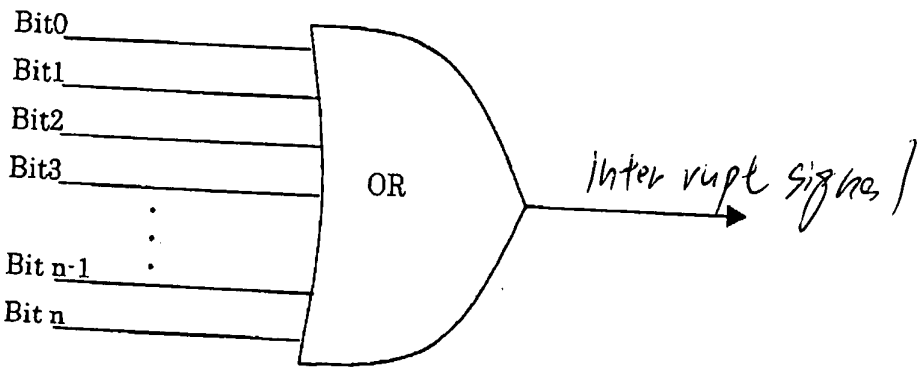


Fig 5

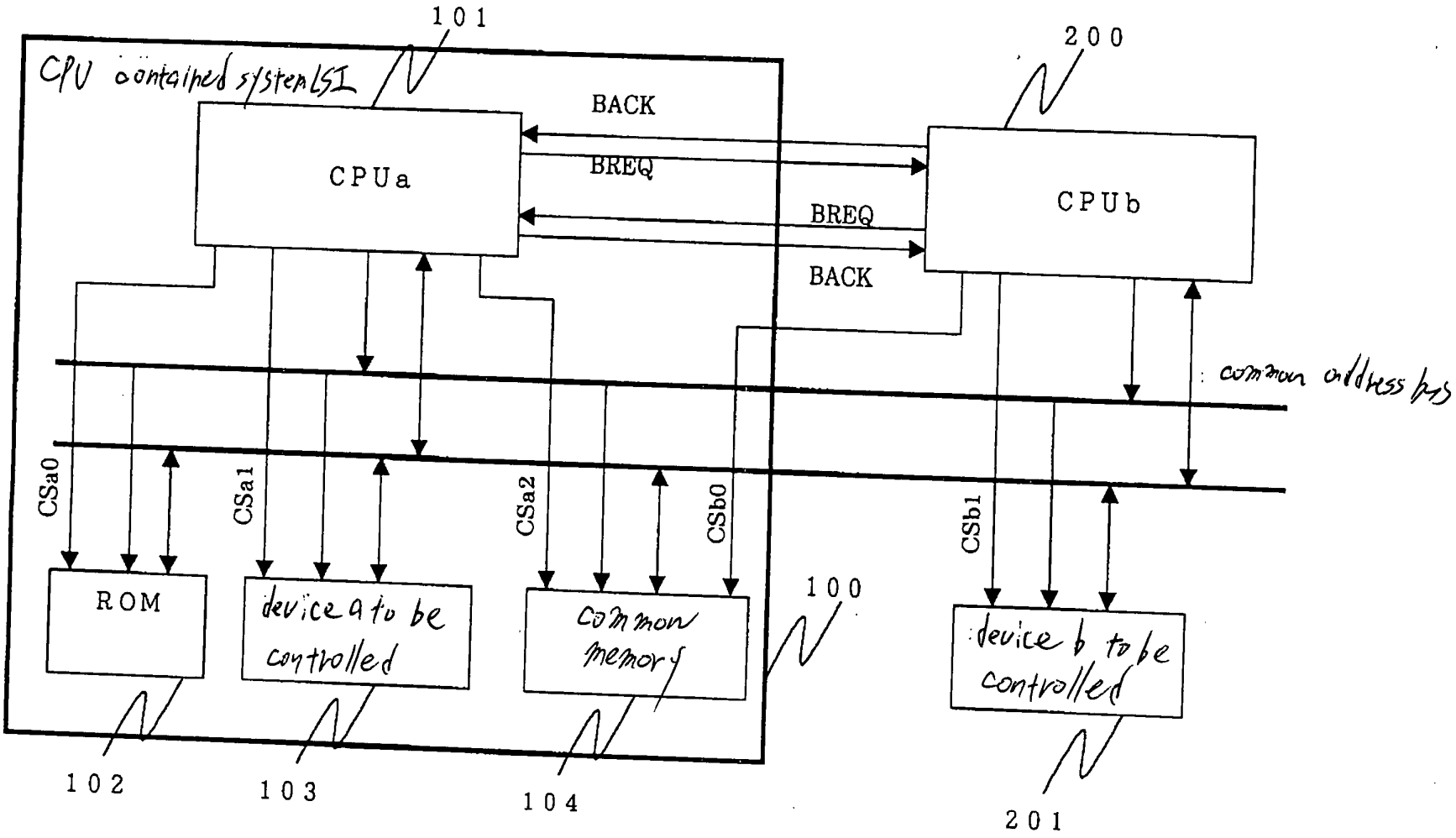

101
CPU contained system LSI
200
BACK
BREQ
BREQ
BACK
CPUa
CPUb
common address bus
CSa0
CSa1
CSa2
CSb0
CSb1
ROM
device a to be controlled
common memory
device b to be controlled
100
102
103
104
201

Fig 6